Docket No.: INTEL-0056 PATENT

AF/ETEN $

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of

Stephen H. TANG et al.

Serial No.: 10/812,894

Filed: 3/31/2003

Confirmation No.: 4982

Group Art Unit: 2827

Examiner: Trong Q. Phan

Customer No.: 68733

For: SRAM DEVICE HAVING FORWARD BODY BIAS CONTROL

TRANSMITTAL OF APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

Submitted herewith is Appellant(s) Appeal Brief in support of the Notice of Appeal filed December 18, 2006. Enclosed is form PTO-2038 for the Appeal Brief fee of $500.00.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
THE FLESHNER GROUP, PLLC

Carl R. Wesolowski
Registration No. 40,372

Attorneys for Intel Corporation

P.O. Box 220898
Chantilly, Virginia 20153-0898
703 766-3701
Date: February 20, 2007

Docket No.: INTEL-0056 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCE

In re Application of	Confirmation No.: 4982
Stephen H. TANG et al.	Group Art Unit: 2827
Serial No.: 10/812,894	Examiner: Trong Q. Phan
Filed: March 31, 2003	Customer No.: 68733

For: SRAM DEVICE HAVING FORWARD BODY BIAS CONTROL

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 223134

Sir:

This appeal is taken from the rejection of claims as set forth in the Office Action of August 18, 2006 (hereinafter the Office Action). In accordance with 37 C.F.R. §41.37, applicant addresses the following items.

REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation. The assignment document is recorded at Reel 015171 and Frame 0332.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

STATUS OF THE CLAIMS

This is an appeal from the final rejection dated August 18, 2006 of claims 1-4, 6-20 and 22-37. No other claims are pending.

STATUS OF AMENDMENTS

All Amendments filed in this application have not been entered. The November 13, 2006 Amendment After Final Rejection that amended an error in claim 3 was not entered, however, all other Amendments were entered. A copy of appealed claims 1-4, 6-20 and 22-37, appears in the attached Claims Appendix.

SUMMARY OF THE CLAIMED SUBJECT MATTER

As stated in 37 C.F.R §41.37(c)(v), applicant is providing the following explanation of each of the independent claims 1, 9 and 18 involved in this appeal. This explanation refers to the specification and drawings. The following is merely an example summary and is not intended to be a discussion of the full and entire scope of the claims. Other interpretations, configurations and embodiments are also within the scope of the pending claims.

In one embodiment, an electronic system (e.g., computer system 10) can include a processor device (e.g., 20) to process data, a static random access memory (SRAM) device (e.g., in memory 40) to store the data and a power control unit (e.g., power control device 27) to control a supply voltage level (e.g., supply line 310) applied to the SRAM device (e.g., 100, 200, 300) and to provide a signal (e.g., 345) indicative of a mode of the SRAM device (such as ACTIVE or INACTIVE/STANDBY).

A SRAM device can have a plurality of memory cells (e.g., 300). Each memory cell

may include a plurality of transistors (e.g., 302, 306 and 313, 316) coupled in an exemplary cross-coupled inverter configuration as shown in Figs. 3 and 5. A switching device (e.g., an NMOS transistor 340) may be coupled to a body of two transistors (e.g., PMOS transistors 302, 312) in the cross-coupled inverter configuration to apply a forward body bias to the transistors (e.g., transistors 302, 312). The power control device 27 may control a supply voltage 310 (e.g., VCC, VCCmin) to a source of each of the transistors (e.g., 302, 312) as well as apply the switching signal 345 (e.g., STANDBY/ACTIVE) to a gate of the transistor 340 based on a mode (e.g., STANDBY mode) of the memory cell 300.

One exemplary NMOS transistor 340 can have a source coupled to a body (e.g., an n-well) of each of the transistors 302 and 312 to apply a forward body bias based on the mode or state of the SRAM device/cell. A drain of the transistor 340 is coupled to GROUND, and a gate of the transistor 340 is coupled to a signal line 345 that receives a signal representing a state or mode of the memory (STANDBY/ACTIVE mode) or portions of the memory. The mode (such as STANDBY/ACTIVE) may be determined and/or controlled by the power control device 27 based on the overall memory (or portions of the memory).

For operations, FIG. 5 also shows a gate of NMOS transistors 320 and 330 coupled to a word line WL (such as WL0 in FIG. 2). A node 305 is selectively connected through the source drain path of the transistor 320 to bitline# 325 (such as bitline b10# in FIG. 2), while the source drain path of the transistor 330 selectively connects node 315 to bitline 335 (such as bitline b10 in FIG. 2). The word line WL drives the gate electrodes of the transistors 320 and 330 in parallel.

The transistor 340 applying the forward body bias to the PMOS transistors 302 and 312 can cause a lower threshold voltage Vt through the body effect. As a result, the inverter characteristics are less skewed towards the NMOS side (as shown in FIG. 4) and the supply voltage (e.g., minimum supply voltage VCCmin) can lowered to allow greater power savings in a STANDBY mode. For example, FIG. 6 shows that the static noise margin increases when the supply voltage is lowered to VCCmin and the body bias is applied to the transistor

302 and 312 of FIG. 5

In another embodiment, another transistor (or similar device) may couple the body of the transistors 302 and 312 to the VCC signal line 310 when the memory is not in the STANDBY mode (ie.g., when the transistor 340 is not turned ON).

Independent Claim 1

Independent claim 1 recites a static random access memory (SRAM) device. For example, Fig. 5 shows a SRAM. The SRAM may include a first and second transistor pair coupled between a supply voltage line and GROUND. For example, Fig. 5 shows an exemplary memory cell may include a plurality of transistors (e.g., 302, 306 and 312, 316) coupled in a cross-coupled inverter configuration between a supply voltage line 310 and GROUND. See also page 7, line 20 to page 8 line 3.

The supply voltage line 310 can receive a first supply voltage based on a first mode of the memory device and to receive a second supply voltage based on a second mode of the memory device, the second supply voltage being different than the first supply voltage. See also VCC, VCCmin, page 8, lines 4-7 and page 9 lines 7-14.

The SRAM may include a first access transistor (320) coupled to a word line (WL), a first bit line (bitline#) and a common node (305) of the second transistor pair (e.g., 302,312) and a second access transistor (330) coupled to the word line (WL), a second bit line (bitline) and a common node (315) of the first transistor pair (e.g., 312, 316). For example, Fig, 5, shows exemplary NMOS transistors 320 and 330 coupled to a word line WL (such as WL0 in FIG. 2), and node 305, 315. See also page 8, lines 8-13.

The SRAM may include a bias transistor (e.g., 340) coupled to a body of one (e.g., 302) of the transistors of the first transistor pair and to a body of one (e.g., 312) of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a non-ACTIVE mode/state. See also, page 8, line 16 to page 9, line 3.

Independent Claim 9

Independent claim 9 recites a SRAM device. The SRAM device may include a first SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration including at least four transistors. For example, Fig. 5 shown a memory cell may include a plurality of transistors (e.g., 302, 306 and 312, 316) coupled in an exemplary cross-coupled inverter configuration.

The SRAM device may include a supply voltage line (e.g., 310) to provide a first supply voltage (e.g., VCC) to two transistors (e.g., sources of transistors 302, 312) of the at least four transistors of the first SRAM memory cell based on a first mode (e.g., ACTIVE)of the first SRAM memory cell and to provide a second supply voltage (e.g., VCCmin) to the two transistors (e.g., sources of transistors 302, 312)based on a second mode (e.g., STANDBY) of the first SRAM memory cell, the second supply voltage being different than the first supply voltage.

The SRAM device may include a switching device (e.g., 340) to apply a forward body bias to the two transistors (e.g., bodies of transistors 302, 312) of the cross-coupled inverter configuration of the first SRAM memory cell. See also page 8, line 19 to page 9, line 3.

Independent Claim 18

Independent claim 18 recites an electronic system. The electronic system (e.g., computer system 10) can include a processor device (e.g., 20) to process data. See Fig. 1.

The electronic system can include a SRAM device to store the data. Fig. 5 shows an exemplary (SRAM) device 300 to store the data.

The electronic system can include a power control unit (e.g., power control device 27) to control a supply voltage level (e.g., 310) applied to the SRAM device and to provide a signal (e.g., 345) indicative of a mode of the SRAM device, the power control unit to apply a first voltage level in a first mode (e.g., VCC in an ACTIVE mode) and to apply a second

voltage level in a second mode (e.g., VCCmin in a STANDBY mode). Figs. 1 and 5 show an exemplary power control device 27 to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device (such as ACTIVE/STANDBY). See page 9, lines 3-9 and page 7, line 3-17.

The electronic system can include a switching device (e.g., 340) in the SRAM device to apply a forward bias to transistors (e.g., a body of transistors 302, 312) within the SRAM device based on the signal (e.g., 345) provided by the power control unit indicative of either the first mode or the second mode of the SRAM device.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 6-20 and 22-37 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,365,475 to Matsumura et al. (hereafter Matsumura) and U.S. Patent 4,567,577 to Oliver. Claims 1-3 and 7-8 form a single group and stand or fall together, and claim 1 is an independent claim. Claims 9-11, 13 and 15-17 form a single group and stand or fall together, and claim 9 is an independent claim. Claims 12, 18-20 and 30 form a single group and stand or fall together, where claim 18 is an independent claim. Claim 4 forms a single group. Claims 6, 14, 22-29 and 31-34 form a single group and stand or fall together. Claims 35-37 form a single group and stand or fall together.

ARGUMENTS

The present application contains three independent claims, namely independent claims 1, 9 and 18. These claims contain different features as may be evidenced by the specifically claimed features and as may be pointed out below. While arguments may be similar for different claims, it should be understood that differently claimed features are expressly used.

Appellants assert that the cited references do not disclose, suggest or render obvious the limitations in the combination of each of claims 1-4, 6-20 and 22-37 of the present application. Appellants respectfully request that all current rejections be withdrawn and that

the decision of the Examiner be reversed based on the following.

35 U.S.C. §103 Rejections

The ultimate determination of obviousness under §103 is a question of law. See, In re Leuders, 111 F.3d 1569, 1571, 42USPQ2d 1481, 1482 (Fed. Cir. 1997). The factual predicates underlying an obviousness determination include the scope and content of the prior art, the differences between the prior art and the claimed invention, and the level of ordinary skill in the art at the time of the invention. See, Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH, 139 F.3d 877, 881, 45 USPQ2d 1977, 1981 (Fed. Cir. 1998).

To reject claims in an application under Section 103, an Examiner must show an unrebutted prima facie case of obviousness. See, In re Deuel, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper prima facie case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. See, In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). It is respectfully submitted that the Examiner has not met the required legal burden as set forth by the courts to substantiate valid rejections under 35 U.S.C. 103(a).

Independent Claim 1

Independent claim 1 recites a first transistor pair coupled between a supply voltage line and GROUND, a second transistor pair coupled between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage based on a first mode of the memory device and to receive a second supply voltage based on a second mode of the memory device, the second supply voltage being different than the first supply voltage. Independent claim 1 also recites a first access transistor, a second access transistor and a bias transistor. The bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward

body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a non-ACTIVE mode/state.

The applied references do not teach or suggest at least these features of independent claim 1. The Office Action states that Matsumura does not teach or suggest the claimed bias transistor as recited in independent claim 1. See page 2, lines 13-15 of Item 2 of the Office Action. The Office Action then relies on Oliver's n-channel transistor 35 (FIG. 2) as corresponding to the claimed bias transistor.

However, Oliver's transistor 35 does not teach or suggest to apply a forward body bias to one of the n-channel transistors 25 or 27. Furthermore, Oliver's transistor 35 does not teach or suggest to apply forward body bias to one of the transistors 25 or 27 based on a non-ACTIVE mode/state.

Despite applicant's previous argument, the Office Action still does not specifically address the claimed features relating to a forward body bias (such as being applied by the alleged transistor 35 in Oliver's FIG. 2).

Forward body bias is a term that is well known to one skilled in the art (and is discussed in the present specification). For example, a forward body bias may occur to an n-channel transistor (such as Oliver's transistors 25 and 27) when a voltage applied to a body of the transistor is higher than a voltage at a source of the transistor. Additionally, with respect to an example in the present specification, a forward body bias may be applied to transistors 302 and 312 (FIG. 5) based on transistor 340 being turned ON (and thereby being coupled to GROUND) and based on sources of the transistors 302 and 312 being coupled to a voltage on VCC signal line 310 (which may vary based on a mode or state of the memory device).

Oliver's transistor 25 (and 27) includes a source coupled to VSS and a drain coupled to a transistor 24 (and ultimately to VDD). The transistor 35 (i.e., the alleged bias transistor) is turned on when the WRITE line 38 is inactive, and then the substrate of the transistor 25 is effectively coupled to VSS (through the transistor 35). Therefore, both the source and substrate of the

transistor 25 are coupled to VSS. Accordingly, there is no suggestion to apply a forward body bias to the transistor 25 (and 27) when the WRITE line 38 is inactive.

Stated differently, a voltage VSS is applied to substrates of the transistors 25 and 27 and a voltage VSS is applied to sources of the transistors 25 and 27. Thus, a substantially same voltage (VSS) is applied to both the source and substrate of the transistors 25 and 27. This does not correspond to a bias transistor to apply a forward body bias (as would be known to one skilled in the art).

The Office Action (on page 3, line 2) also states that Oliver's transistor 35 applies a forward negative bias voltage VSS to the transistors 25 and 27. However, the terminology of a forward negative bias voltage is never used in Oliver. Applicant respectfully submits that there is no basis for the naming of the voltage VSS as "forward negative." Oliver does not apply a forward body bias based on WRITE line 38 being inactive.

Further, the Office Action appears to have incorrectly described Oliver's disclosure. For example, the Office Action appears to state the applying of voltage VSS to the substrate of the transistors 25/27 is called a body effect and that Oliver uses a back gate bias to control the transistors. The terminology of the back gate bias and body effect is described at col. 3, lines 14-20. However, this terminology is discussed with respect to the transistor 36 being turned on (and the transistor 35 being off). See col. 3, lines 10-14. Stated differently, the body effect is based on a WRITE line 38 being active (and not the WRITE line 38 being inactive). Thus, the Office Action's reference to body effect and/or back gate bias appears to be improper.

The Office Action further identifies the body effect during a non-active WRITE mode/state as motivation to combine Matsumura and Oliver. However, the alleged body effect occurs when the WRITE line 38 is active (and thus not when the WRITE signal being inactive). Thus, the Office Action's alleged motivation actually teaches away from the claimed features. The Office Action therefore does not provide proper motivation to combine Matsumura and Oliver.

There is no suggestion to combine Matsumura and Oliver as alleged in the Office Action. That is, Matsumura relates to different voltages (V1, V2) being applied to p-channel transistors 21 and 22. See Matsumura's FIG. 3. In contrast, Oliver applies constant voltages VSS and VDD as well as applies a voltage VSS to the substrate of the n-channel transistors 25 and 27. There is no suggestion of how to combine Oliver's voltage VSS being applied to substrate of the n-channel transistors with Matsumura's p-channel transistors that receive voltages V1/V2. These are different principles of operations (and there is no suggestion in the prior art to combine those principles). Additionally, there is no suggestion in the prior art to modify Matsumura so as to include providing a varying potential to substrates of transistors (such as is alleged within Oliver). The only suggestion for the claimed features is provided in applicants' own specification. The Office Action clearly relies on impermissible hindsight by relying on applicants' own specification in order to combine Matsumura and Oliver. The Office Action therefore fails to make a prima facie case of obviousness.

For at least the reasons set forth above, the applied references do not teach or suggest all the features of independent claim 1. Thus, independent claim 1 defines patentable subject matter.

Dependent Claim 4

The Office Action states that Matsumura does not teach or suggest the claimed bias transistor as recited in independent claim 1. See page 2, lines 13-15 of Item 2 of the Office Action.

Dependent claim 4 recites the bias transistor applies the forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a mode of the memory device. Oliver does not teach or suggest that the transistor 35 applies a forward body bias based on a mode of the memory device. That is, a WRITE line being inactive is not a mode of a memory device. Dependent claim 4 defines patentable subject matter at least for this additional reason.

Dependent Claims 6, 14, 22-29 and 31-34

The Office Action states that Matsumura does not teach or suggest the claimed bias transistor as recited in independent claim 1. See page 2, lines 13-15 of Item 2 of the Office Action.

Dependent claim 6 recites a gate of the bias transistor is coupled to a signal line to receive a STANDBY signal indicative of a STANDBY state of the memory device.

The Office Action appears to state that the WRITE line being inactive is inherently present only during a non-ACTIVE WRITE mode/state. However, as stated in MPEP §2112, to establish inherency, the evidence must make clear that the missing matter is necessarily present in the thing described in the reference. The mere fact that a certain thing may result for a given set of circumstances is not sufficient. Oliver's WRITE line being inactive does not necessarily correspond to a STANDBY signal indicative of a STANDBY state of a memory device. This is, the present application clearly describes a STANDBY signal and a STANDBY state of a memory device. One skilled in the art would clearly know that Oliver's WRITE line signal, or lack of the WRITE line signal, does not necessarily correspond to a STANDBY signal indicative of a STANDBY state of a memory device. Rather, Oliver's WRITE line signal merely relates to whether data is being written. The lack of a WRITE line signal does not necessarily correspond to a STANDBY state of a memory device. Therefore, the claimed features are not inherent.

In the December 6, 2006 Advisory Action, the STANDBY state of the memory device appears to be correlated to the WRITE line 38 being inactive. See Item 11 of the December 6, 2006 Advisory Action. As described above, when the WRITE line 38 is inactive, the transistor 35 causes transistors 25, 27 "to function as normal ... devices." See column 3 lines 7-9 of Oliver. When the WRITE line 38 is active, the transistor 36 operates to turn off transistors 25, 27 thereby "allowing ... charges at nodes 23 and 30 to be placed into the latch without having to ... overpower the previous state of the latch." See column 3 lines 16-20 of Oliver. Thus, Oliver does not teach or suggest that the transistor 35 applies a forward body bias. Further,

Oliver does not teach or suggest that the transistor 35 applies a forward body bias when the WRITE line 38 is inactive. Further, Oliver does not teach or suggest operations of transistors 35, 36 with respect to a mode of a memory device. That is, a WRITE line being inactive is not a mode of a memory device.

For at least the reasons set forth above, the applied references do not teach or suggest features recited in dependent claim 6. Thus, dependent claim 6 defines patentable subject matter for at least for this additional reason.

Each of dependent claims 14, 22-29 and 31-34 also relate to a STANDBY mode. Oliver does not teach or suggest these features for at least the reasons set forth above. Each of these dependent claims defines patentable subject matter at least for this additional reason.

Dependent Claims 35-37

Dependent claim 35 recites wherein the first supply voltage and the second supply voltage are applied to a source of the one transistor of the first transistor pair and to a source of the one transistor of the second transistor pair.

Oliver discloses constant voltage VDD being applied to transistors 24, 29 and constant voltage VSS being applied to sources of transistors 25, 27. See Figs. 1-2 of Oliver.

The December 6, 2006 Advisory Action appears to state that Matsumura discloses different supply voltages V1, V2 and respective GROUND G1 different form G2. See Item 11 of the December 6, 2006 Advisory Action. In contrast, Appellants note that Matsumura discloses supply line V1 equal to supply line V2 when applied to sources of both the transistors 25 and 27. See for example Figs. 17, 4, 5A, 5B of Matsumura. When supply line V1 does not equal supply line V2 or ground line G1 doesn't equal ground line G2, Matsumura appears to disclose the lines being individually applied to respective sources of transistors 25 and 27 or transistors 24 and 29 where one of the lines has a fixed value (e.g., V1) and the other is variable (e.g., V2). See Figs. 5A-7D of Matsumura.

For at least the reasons set forth above, the applied references do not teach or suggest features recited in dependent claim 35. Thus, dependent claim 35 defines patentable subject matter for at least for this additional reason.

Each of these dependent claims 36-37 define patentable subject matter at least for this additional reason.

Independent Claim 9

Independent claim 9 recites a SRAM device including a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell.

The Office Action states that Matsumura does not teach or suggest the claimed switching device recited in claim 9. See page 2, lines 13-15 of Item 2 of the Office Action. The Office Action then relies on Oliver's n-channel transistor 35 (FIG. 2) as corresponding to the claimed switching device.

However, Oliver's transistor 35 does not teach or suggest to apply a forward body bias to one of the n-channel transistors 25 or 27. Furthermore, Oliver's transistor 35 does not teach or suggest to apply forward body bias to one of the transistors 25 or 27 based on a non-ACTIVE mode/state.

Forward body bias is a term that is well known to one skilled in the art (and is discussed in the present specification). For example, a forward body bias may occur to an n-channel transistor (such as Oliver's transistors 25 and 27) when a voltage applied to a body of the transistor is higher than a voltage at a source of the transistor.

Oliver's transistor 25 (and 27) includes a source coupled to VSS and a drain coupled to a transistor 24 (and ultimately to VDD). The transistor 35 (i.e., the alleged bias transistor) is turned on when the WRITE line 38 is inactive, and then the substrate of the transistor 25 is effectively coupled to VSS (through the transistor 35). Therefore, both the source and substrate of the

transistor 25 are coupled to VSS. Accordingly, there is no suggestion to apply a forward body bias to the transistor 25 (and 27) when the WRITE line 38 is inactive.

Further, the Office Action appears to have incorrectly described Oliver's disclosure. For example, the Office Action appears to state the applying of voltage VSS to the substrate of the transistors 25/27 is called a body effect and that Oliver uses a back gate bias to control the transistors. The terminology of the back gate bias and body effect is described at col. 3, lines 14-20. However, this terminology is discussed with respect to the transistor 36 being turned on (and the transistor 35 being off). See col. 3, lines 10-14. Stated differently, the body effect is based on a WRITE line 38 being active (and not the WRITE line 38 being inactive). Further, Oliver teaches to turn off transistors 25, 27 using transistor 36 when WRITE line 38 is active. Accordingly, the Office Action's reference to body effect and/or back gate bias appears to be improper. Thus, even if combined, the applied references do not teach features of switching device and combinations thereof as recited in claim 9.

The Office Action further identifies the body effect during a non-active WRITE mode/state as motivation to combine Matsumura and Oliver. However, the alleged body effect occurs when the WRITE line 38 is active (and thus not when the WRITE signal being inactive). Thus, the Office Action's alleged motivation actually teaches away from the claimed features. The Office Action therefore does not provide proper motivation to combine Matsumura and Oliver.

There is no suggestion to combine Matsumura and Oliver as alleged in the Office Action. That is, Matsumura relates to different voltages (V1, V2) being applied to p-channel transistors 21 and 22. See Matsumura's FIG. 3. In contrast, Oliver applies constant voltages VSS and VDD, as well as applies a voltage VEE to the substrate of the n-channel transistors 25 and 27 when the WRITE line 38 is active and the voltage VSS to the substrate of the n-channel transistors 25 and 27 otherwise. There is no suggestion of how to combine Oliver's voltage being applied to substrate of the n-channel transistors with Matsumura's p-channel transistors that receive voltages V1/V2. These are different principles of operations (and there is no suggestion in the

prior art to combine those principles). Additionally, there is no suggestion in the prior art to modify Matsumura so as to include providing a varying potential to substrates of transistors (such as is alleged within Oliver). The only suggestion for the claimed features is provided in applicants' own specification. The Office Action clearly relies on impermissible hindsight by relying on applicants' own specification in order to combine Matsumura and Oliver. The Office Action therefore fails to make a prima facie case of obviousness.

For at least the reasons set forth above, the applied references do not teach or suggest features recited in independent claim 9. Thus, independent claim 9 defines patentable subject matter.

Independent Claim 18

Independent claim 18 recites a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the power control unit to apply a first voltage level in a first mode and to apply a second voltage level in a second mode, the SRAM device including a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit indicative of either the first mode or the second mode of the SRAM device.

The Office Action states that Matsumura does not teach or suggest the claimed switching device recited in claim 18. See page 2, lines 13-15 of Item 2 of the Office Action. The Office Action then relies on Oliver's n-channel transistor 35 (FIG. 2) as corresponding to the claimed switching device.

However, Oliver's transistor 35 does not teach or suggest to apply a forward body bias to one of the n-channel transistors 25 or 27. Furthermore, Oliver's transistor 35 does not teach or suggest to apply forward body bias to one of the transistors 25 or 27 based on a non-ACTIVE mode/state.

Forward body bias is a term that is well known to one skilled in the art (and is discussed in the present specification). For example, a forward body bias may occur to an n-channel

transistor (such as Oliver's transistors 25 and 27) when a voltage applied to a body of the transistor is higher than a voltage at a source of the transistor.

Oliver's transistor 25 (and 27) includes a source coupled to VSS and a drain coupled to a transistor 24 (and ultimately to VDD). The transistor 35 (i.e., the alleged bias transistor) is turned on when the WRITE line 38 is inactive, and then the substrate of the transistor 25 is effectively coupled to VSS (through the transistor 35). Therefore, both the source and substrate of the transistor 25 are coupled to VSS. Accordingly, there is no suggestion to apply a forward body bias to the transistor 25 (and 27) when the WRITE line 38 is inactive.

Further, the Office Action appears to have incorrectly described Oliver's disclosure. For example, the Office Action appears to state the applying of voltage VSS to the substrate of the transistors 25/27 is called a body effect and that Oliver uses a back gate bias to control the transistors. The terminology of the back gate bias and body effect is described at col. 3, lines 14-20. However, this terminology is discussed with respect to the transistor 36 being turned on (and the transistor 35 being off). See col. 3, lines 10-14. Stated differently, the body effect is based on a WRITE line 38 being active (and not the WRITE line 38 being inactive). Further, Oliver teaches to turn off transistors 25, 27 using transistor 36 when WRITE line 38 is active. The Office Action's reference to body effect and/or back gate bias appears to be improper.

Additionally, Oliver clearly does not suggest to apply a forward body bias based on a signal provided by a power control unit (that also applies a first voltage level in a first mode and applies a second voltage level in a second mode). Thus, even if combined, the applied references do not teach features of switching device and combinations thereof as recited in claim 18.

The Office Action further identifies the body effect during a non-active WRITE mode/state as motivation to combine Matsumura and Oliver. However, the alleged body effect occurs when the WRITE line 38 is active (and thus not when the WRITE signal being inactive). Thus, the Office Action's alleged motivation actually teaches away from the claimed features. The Office Action therefore does not provide proper motivation to combine Matsumura and Oliver.

There is no suggestion to combine Matsumura and Oliver as alleged in the Office Action. That is, Matsumura relates to different voltages (V1, V2) being applied to p-channel transistors 21 and 22. See Matsumura's FIG. 3. In contrast, Oliver applies constant voltages VSS and VDD, as well as applies a voltage VEE to the substrate of the n-channel transistors 25 and 27 when the WRITE line 38 is active and the voltage VSS to the substrate of the n-channel transistors 25 and 27 otherwise. There is no suggestion of how to combine Oliver's voltage being applied to substrate of the n-channel transistors with Matsumura's p-channel transistors that receive voltages V1/V2. These are different principles of operations (and there is no suggestion in the prior art to combine those principles).

Also, there is no suggestion to combine Matsumura and Oliver so as to relate to the specifically claimed features of the power control unit recited in claim 18. The only suggestion for the claimed features is provided in applicants' own specification. The Office Action clearly relies on impermissible hindsight by relying on applicants' own specification in order to combine Matsumura and Oliver. The Office Action therefore fails to make a prima facie case of obviousness.

For at least the reasons set forth above, the applied references do not teach or suggest features recited in independent claim 18. Thus, independent claim 18 defines patentable subject matter.

Additionally, dependent claim 12 recites the switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to the power control unit. Dependent claim 12 defines patentable subject matter at least for this additional reason similar to claim 18.

CLAIMS APPENDIX

The attached Claims Appendix contains a copy of the claims involved in the appeal.

EVIDENCE APPENDIX

Applicant has not provided any evidence with this appeal and therefore an Evidence Appendix is not provided.

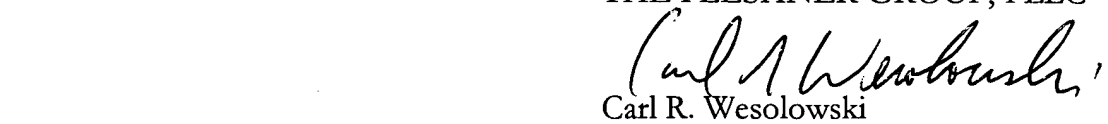
RELATED PROCEEDINGS APPENDIX

Applicant is not providing copies of related decisions and therefore a Related Proceeding Appendix is not provided.

CONCLUSION

It is respectfully submitted that the above arguments show that each of claims 1-4, 6-20 and 22-37 are patentable over the applied references. Based at least on these reasons, it is respectfully submitted that each of claims 1-4, 6-20 and 22-37 defines patentable subject matter. Applicant respectfully requests that the rejections of claims 1-4, 6-20 and 22-37 set forth in the August 18, 2006 Office Action be withdrawn.

Respectfully submitted,
THE FLESHNER GROUP, PLLC



Carl R. Wesolowski
Registration No. 40372

Attorneys for Intel Corporation

P. O. Box 220898
Chantilly, Virginia 20153-0898
703 766-3701
Date: February 20, 2007
Please direct all correspondence to Customer Number 68733
Document in ProLaw

CLAIMS APPENDIX

Listing of Claims:

1. (Previously Presented) A static random access memory (SRAM) device comprising:

a first transistor pair coupled between a supply voltage line and GROUND;

a second transistor pair coupled between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage based on a first mode of the memory device and to receive a second supply voltage based on a second mode of the memory device, the second supply voltage being different than the first supply voltage;

a first access transistor coupled to a word line, a first bit line and a common node of the second transistor pair;

a second access transistor coupled to the word line, a second bit line and a common node of the first transistor pair; and

a bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a non-ACTIVE mode/state.

2. (Original) The SRAM device of claim 1, wherein the bias transistor comprises an NMOS transistor having a source coupled to GROUND.

3. (Previously Presented) The SRAM device of claim 2, wherein a source of the bias transistor is coupled to the body of the one transistor of the first transistor pair and to the body of the one transistor of the second transistor pair.

4. (Previously Presented) The SRAM device of claim 1, wherein the bias transistor applies the forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a mode of the memory device.

5. (Canceled)

6. (Original) The SRAM device of claim 1, wherein a gate of the bias transistor is coupled to a signal line to receive a STANDBY signal indicative of a STANDBY state of the memory device.

7. (Original) The SRAM device of claim 1, wherein the bias transistor turns ON based on a STANDBY signal applied to a gate of the bias transistor.

8. (Original) The SRAM device of claim 1, wherein the one transistor of the first transistor pair comprises a PMOS transistor and the one transistor of the second transistor pair comprises another PMOS transistor.

9. (Previously Presented) A static random access memory (SRAM) device comprising:

a first SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration including at least four transistors;

a supply voltage line to provide a first supply voltage to two transistors of the at least four transistors of the first SRAM memory cell based on a first mode of the first SRAM memory cell and to provide a second supply voltage to the two transistors based on a second mode of the first SRAM memory cell, the second supply voltage being different than the first supply voltage; and

a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell.

10. (Previously Presented) The SRAM device of claim 9, further comprising a power control unit to change the supply voltage on the supply voltage line based on either the first mode or the second mode of the first SRAM memory cell.

11. (Previously Presented) The SRAM device of claim 10, wherein the power control unit further to control switching of the switching device based on either the first mode or the second mode of the first SRAM memory cell.

12. (Original) The SRAM device of claim 10, wherein the switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to the power control unit.

13. (Previously Presented) The SRAM device of claim 12, wherein a drain of the NMOS transistor is coupled to a body of each of the two transistors of the at least four transistors of the first SRAM memory cell.

14. (Previously Presented) The SRAM device of claim 12, wherein a gate of the NMOS transistor receives a STANDBY signal from the power control unit indicative of a STANDBY state of the first SRAM memory cell.

15. (Previously Presented) The SRAM device of claim 12, wherein the NMOS transistor turns ON based on a STANDBY signal applied to the gate of the NMOS transistor.

16. (Previously Presented) The SRAM device of claim 9, further comprising a second SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration of the second SRAM memory cell including at least four transistors, the supply voltage line to provide a supply voltage to two transistors of the at least four transistors of the second SRAM memory cell based on a mode of the second SRAM memory cell.

17. (Previously Presented) The SRAM device of claim 16, wherein the switching device to apply a forward body bias to the two transistors of the at least four transistors of the cross-coupled configuration of the second SRAM memory cell.

18. (Previously Presented) An electronic system comprising:
a processor device to process data;
a static random access memory (SRAM) device to store the data; and
a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the power control unit to apply a first voltage level in a first mode and to apply a second voltage level in a second mode, the SRAM device including:
a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit indicative of either the first mode or the second mode of the SRAM device.

19. (Original) The electronic system of claim 18, wherein the switching device applies the forward body bias by coupling a body of each of the transistors to GROUND.

20. (Original) The electronic system of claim 18, wherein applying the forward bias to the transistors increases a static noise margin.

21. (Canceled)

22. (Previously Presented) The electronic system of claim 18, wherein the second mode comprises a STANDBY mode and the first mode comprises an ACTIVE mode.

23. (Previously Presented) The electronic system of claim 22, wherein the switching device to apply the forward body bias in the STANDBY mode.

24. (Previously Presented) The electronic system of claim 23, wherein the power control unit to provide the supply voltage level to two transistors of the SRAM device in both the STANDBY mode and the ACTIVE mode.

25. (Previously Presented) The electronic system of claim 24, wherein the SRAM device further including a device to couple bodies of the two transistors of a memory cell in the SRAM device to a supply voltage line when the memory cell is not in the STANDBY mode.

26. (Previously Presented) The SRAM device of claim 17, wherein the switching device to apply the forward body bias to the two transistors of the at least four transistors of the second SRAM memory cell when the second SRAM memory cell is in a STANDBY mode.

27. (Previously Presented) The SRAM device of claim 9, wherein the second mode comprises a STANDBY mode and the first mode comprises an ACTIVE mode.

28. (Previously Presented) The SRAM device of claim 27, wherein the switching device to apply the forward body bias in the STANDBY mode.

29. (Previously Presented) The SRAM device of claim 28, further comprising a device to couple bodies of the two transistors of the at least four transistors to the supply voltage line when the first SRAM memory cell is not in the STANDBY mode.

30. (Previously Presented) The SRAM device of claim 1, wherein the supply voltage line applies the first supply voltage in the first mode and applies the second supply voltage in the second mode.

31. (Previously Presented) The SRAM device of claim 30, wherein the second mode comprises a STANDBY mode and the first mode comprises an ACTIVE mode.

32. (Previously Presented) The SRAM device of claim 31, wherein the bias transistor to apply the forward body bias in the STANDBY mode.

33. (Previously Presented) The SRAM device of claim 32, wherein the supply voltage line to provide a supply voltage to the one transistor of the first transistor pair and the one transistor of the second transistor pair in both the STANDBY mode and the ACTIVE mode.

34. (Previously Presented) The SRAM device of claim 33, further comprising a device to couple bodies of the two transistors to the supply voltage line when a memory cell of the SRAM device is not in the STANDBY mode.

35. (Previously Presented) The SRAM device of claim 1, wherein the first supply voltage and the second supply voltage are applied to a source of the one transistor of the first transistor pair and to a source of the one transistor of the second transistor pair.

36. (Previously Presented) The SRAM device of claim 9, wherein the supply voltage line to provide the first supply voltage and the second supply voltage to sources of the two transistors of the at least four transistors of the first SRAM memory cell.

37. (Previously Presented) The electronic system of claim 18, wherein the power control unit to apply the first voltage level and the second voltage level to sources of transistors within the SRAM device.